AMENDMENTS TO THE SPECIFICATION

Amend the first full paragraph on page 16 as follows:

The row selecting signal is applied to a data line directly connected to the gate electrodes of the ferroelectric gate FETs of the same row, and the row selection for writing is performed. Also, the data signal is connected to the source electrodes of the ferroelectric gate FETs of the same column, and the data (voltage) for varying the conducting state (conducting or non-conducting) of the ferroelectric gate FET in synchronization with the row selection is applied. In this manner, data writing is performed

Amend the paragraph bridging pages 26-27 as follows:

The source electrodes of the first ferroelectric gate FETs (Tr1) in the same column are connected together and data signal $V_{b(m)}$ or $V_{b(m+1)}$ is input in a column unit. Likewise, the source electrodes of the second ferroelectric gate FETs (Tr2) In the same column are connected together and the data signal $V_{b(m)}$ or $V_{b(m+1)}$ is input in a column unit. Also, the gate electrodes of the first ferroelectric gate FETs (Tr1) in the same row are interconnected and row selecting signal $V_{g(n)}$ or $V_{g(n+1)}$ is input in a row unit via a data line directly connected to gates of the respective ferroelectric gate transistors. Furthermore, the gate electrodes of the second ferroelectric gate FETS (Tr2) in the same row are interconnected and the row selecting signal $V_{g(n)}$ or $V_{g(n+1)}$ is input in a row unit. The pixel electrode 1 of each pixel is connected to the drains of the first and second ferroelectric gate FETs (Tr1 and Tr2), and voltage Vcom is applied to the counter electrode 2. A description will hereinafter be made of the drive method in this constitution.